IDENTIFICATION OF THE PROBLEM

At the present time there is a need for more powerful supercomputers. [2] By mapping software into hardware, optimal speed of execution can be achieved. Fast sequential operations will result since the conditional branch structure of every program is to be embedded in hardware. Logic functions are also directly embedded in hardware so long strings of sequential logic functions do not even have to be clocked and speed of execution is dependent upon the technology used to make the devices. This bypasses (for that part of the problem where it applies) the Flynn Limit, one of the main bottlenecks in modern computing.[3] Since there is no need to fetch instructions from memory because there are no instructions to fetch (they're all embedded in the hardware) and since data most is localized and not on a bus, the Von Neumann bottleneck [4] is reduced to the much simpler problem of some process or processes getting to the data needed. Since all global data is kept to an optimized minimum, any kind of bus contention is reduced.

In supercomputing there are many different architectures being tried, for example, large vector processors, highly parallel processors, RISC processors, and the systolic array approach. [2,5,6,7] Some have as bottlenecks memory fetches and some kind of sequencer decoding scheme. Some solutions use compiler technology to reprogram the microcode for highly recursive or highly used portions of the program. All these approaches still have a processor or processors that have to fetch operational code from memory and execute that code. And all force a high level language to be chopped into a large number of smaller "machine language" steps.

The research proposed will look for a solution to the throughput problem by completely reconfiguring the hardware of the computer to reflect the software being run.

The ability to completely reprogram the computer's hardware means that this new architecture can emulate any of the above computer architectures and run object code compiled for that computer. Programmable devices have already been used to implement a Cray compatible minisupercomputer. [8]

There have been some attempts to put a software algorithm into hardware, the most notable being Zycad Corp. of Minneapolis,

Minnesota. In the computationally intensive world of logic and fault simulation Zycad has managed to implement, in hardware, a logic algorithm (the System Development Engine-hereafter "SDE") that runs faster than similar algorithms implemented on a Cray supercomputer. Zycad uses ECL PALs for the SDE. The SDE has a throughput, not measured in MIPS or MFLOPs but in events per seconds, of one billion events per second, the average event on a conventional computer takes about 200 instructions. Conservatively we can say that the SDE runs at somewhere around 100 BIPS (billion instructions per second) [9] although, to drive a point home, there are no instructions being executed in the conventional sense. Zycad also features a fault simulator whose algorithm is embedded in programmable array logic (PALs): this is the fastest of the hardware fault evaluators. This trend to solve the speed issue by making a single purpose computer (as opposed to a general purpose computer) is just becoming a cost effective solution for computationally intensive problems. However, the concept of hardware that is dynamically reconfigurable to suit any of a large number of algorithms can produce the benefits of both.

There are two main thrusts to the proposed research

1) Develop the hardware portion of the computer by studying the boundary problem, ie. how to connect many programmable gate-arrays to allow program flow across multiple devices.

2) Create a compiler that will take any construct of a high level language, in this case C, and produce the relevant programming for the configuration of the device topology resulting from part 1.

The main thrust of this Phase I proposal will be to study a basic overlapping cell topology of seven of the reconfigurable devices to determine the speed and the percent utilization of the devices for each construct of the C language.

BACKGROUND AND TECHNICAL APPROACH

Logic Cell Arrays (hereafter LCAs) are already being used in design verification of gate array and standard cell projects. By emulating the proposed design in a breadboard environment system considerations can be addressed with confidence. [10,11] There is also a worldwide search to identify computationally intensive areas and implement these in hardware. The Japanese have proposed The Sparse Matrix Solving Machine, The Relational Database Machine [12,13] and other computationally intensive algorithms to be put in hardware. Other examples of more familiar algorithms implemented in hardware are the high speed multiplier chip, the vector multiplier and interrupt handlers and of course every instruction in every computer (it is well known that all logic and arithmetic operations can be carried out by the NAND function).

Hardware reconfiguration is already being used to some degree in the supercomputer community. The GF11 supercomputer uses the Memphis switch in its SIMD architecture to completely rearrange interconnections between its 576 20-MFLOP processors. [13] The Transputer is another well known example of a highly reconfigurable hardware scheme. [14]

By using large numbers of the totally reconfigurable fully programmable LCAs, research can be done on different computer architectures not by simulating or emulating the design but by actually implementing the design in a matter of micro-seconds [1]. This design would be able to be changed at any time. Trouble shooting will be an easy job because direct contact can be had to the inside of any function that is being tested.

A. S. Tanenbaum put it nicely, "Hardware and software are logically equivalent. Any operation performed by software can also be built directly into hardware and any instruction executed by the hardware can also be simulated in software. The decision to put certain features in hardware and others in software is based on such factors as cost, speed, reliability and frequency of change. There are no hard and fast rules to the effect that X must go into hardware and Y must be programmed explicitly. Designers with different goals may, and often do, make different decisions... the boundary between hardware and software is arbitrary and constantly changing. Today's software is tomorrow's hardware, and vice versa.". [15]

Since the cost of putting software into hardware has fallen dramatically it is our opinion that it is now feasible to put all software into hardware thereby creating the most flexible computer ever made.

ANTICIPATED BENEFITS OF RESULTS

The benefits of building a fully programmable reconfigurable hardware architecture will be seen in many fields. A completely reconfigurable architecture has obvious applications in the area of simulation. Whatever circuit is under consideration can be loaded directly in hardware and a functional simulation can be done in real time. A full timing simulation could be done by appropriate routing for different time delays. This computer could be a testbed for implementing different computer architectures by fully reconfiguring the hardware to be that architecture. It could implement some architecture with any kind of DSP (digital signal processing) conceivable.

The computer could also function in the manner proposed, that is as a fully programmable reconfigurable hardware engine. This would allow program flow to be optmized in hardware for every program which we believe would be a major breakthrough in the supercomputing arena.

PHASE I RESEARCH OBJECTIVES

The specific technical objectives of this Phase I research are:

1) To show by construction that software can be mapped directly into hardware.

2) To develop the LCA array interconnections and memory interface definition.

3) To provide calculations to show what the throughput will be in a larger configuration.

The proof by construction for 1 will consist of using The XACT Development System offered by Monolithic Memories [1] to show that it is possible to map software into hardware. Using this information it is possible to develop a compiler that would take

the C programming language into the binary files needed to program the LCAs directly (One of the main thrusts of the Phase II part of this project).

The development of the interconnection network for 2 will be for a small number of LCAs and a small amount of memory and be downloaded by the XACT Development System. This will be the basis of a much larger system to be developed later under Phase II.

The calculations to be performed in 3 will be to determine the speed of execution of the C constructs that have been translated into the hardware. These calculations will be used if a Phase II grant is sought.

PHASE I RESEARCH PLAN

On the XACT development system The Imagination Works will endeavor to show that there is a translation of each construct of C into an electronic circuit. The XACT system will translate the circuit into the appropriate binary files to be downloaded into the LCAs. Under control of the XACT system, simulation RESULTS will be obtained to confirm the proper execution of the translated C constructs. Then the information generated by the XACT system can then be downloaded to the LCAs to confirm the actual transformation from a software module into a hardware engine. A chart will be made showing the execution times of the various constructs. Another chart will be created showing the number of LCA primitives it takes to implement the given construct. From these two charts one would be able to determine whether or not programs of any size and complexity could be translated into a buildable supercomputer. This could also answer the question of the hardware/software tradeoff problem. [16] Since any combination of hardware or software could be loaded into the computer one could have an all hardware solution or a mostly software (with any choice of architecture) solution and compare the resulting performance of each approach. Then by putting different functions into or out of hardware a hardware to software tradeoff graph could be produced. The C functions will be limited to (yet made general enough for expansion) 8 bit arguments to facilitate research. C functions such as multiplication and division may be omitted from this Phase I research unless time permits their implementation.

The actual topography of the interconnections shall be a very simple overlapping approach. The LCAs I/O ports will be divided into five sections which will consist of four sections with an equal number of I/O ports ('corners'), and a fifth area ('vortex port') to be connected to either memory or some sort of general I/O port. The the size of the vortex port will be a factor of the size of the computer, ie. how many LCAs there are. In a configuration to be used in the proposed research there would be seven LCAs with a total of 406 uncommitted I/O ports. If we allow the corner groups to have 11 members each this would leave 14 for the vortex port (96 pins for total computer I/O). These ports could have many kinds of devices interfaced through them to the computer such as high speed multipliers, digital signal processors or local memory. The four corner ports of each device will link to four other devices at the corners of the respective devices. Devices on the topological boundary of the computer will have unused corner ports these can be left unused or routed to other boundary LCAs.

All calculations to be made will be based on a worst case timing, worst case routing, and worst case process(of the silicon itself). calculations for critical path delay for each translation of the programming constructs into hardware, for number of cycles per construct, and LCA primitive usage will be included in the final report. To confirm that the calculated results are accurate the data taken from simulation runs will be used to verify statistically the accuracy of the calculations.

The array to be used is MMI's M2064-50 LCA, a 2K gate equivalent array with 58 fully programmable I/O pins. The research shall take as the main tool for investigation the XACT Development System, P-SILOS Simulation Package, LCA in-circuit Emulator Pod, and XACT Evaluation Kit. [1] These development tools should be enough to complete proposed research for Phase I. By allowing up to seven LCAs to be serviced at once this shall provide enough basic units to allow a generalization to be made with regard to the manufacture of a more involved system.

STATEMENT OF WORK

1) Project Objective

The contractor shall provide a detailed description of the architecture of the proposed new supercomputer. Provided as well will be: the detailed electronic schematic diagrams for each C function, the calculations showing

1.1) The percent utilization of the C function in number of LCA primitives.

1.2) The worst case timing path analysis for each C function.

2) Work to be performed on the following tasks:

2.1) Definition of supercomputer architecture.

2.2) Implementation of the C functions in schematic representation.

2.3) Calculation of utilization.

2.4) Calculation of worst case timing.

2.5) Preparation of final report.

3) Performance Schedule

Task 2.1 completed two months after start of work.
Task 2.2 completed five months after start of work.
Task 2.3 completed five months after start of work.
Task 2.4 completed five months after start of work.
Task 2.5 completed six months after start of work.

4) Deliverable

The contractor shall provide a Final Report containing the data from the experimental work of Tasks 2.1 through 2.5 and include any graphs or charts generated by such work.

5) Facilities/Equipment

The equipment required for this work consists of:

The LCA Development System
The LCA Simulator - P-SILOS
The LCA In-Circuit-Emulator
The LCA In-Circuit-Emulator Pod
An IBM-AT compatible personal computer

The Imagination Works needs only the first four items (see attached budget)

The Imagination Works offices occupy approximately 400 square feet located at 18622 Saticoy Reseda, CA 91335.

RELATED WORK

During the last two years the principal investigator has been involved in IRAD work on state-of-the-art semiconductor manufacturer evaluation, investigating speed vs. feature size for use in an advanced MIL-STD-1750A custom chip set. Simultaneous ongoing investigation into hardware accelerators for logic and fault evaluation has kept the principal investigator abreast of the most current advanced in the semiconductor industry.

KEY PERSONNEL BACKGROUND

As principal investigator, Steven M. Casselman, is well suited to carry out the proposed research. For the last two years he has been a design engineer at Teledyne Systems Company. As a graduate of mathematics from UCLA and an electronic design engineer, Mr. Casselman has a knowledge of both the hardware involved and the topology of the problem. The Imagination Works has released a product, The Environment (an innovative user-friendly shell), written by Mr. Casselman entirely in C.

Involved in the IRAD program at Teledyne for the last year Mr. Casselman has traveled to gate-array vendors and computer aided engineering manufacturers to research tradeoff and current trend studies. Versed in the arts of digital modelling, behavioral modelling, and large system simulations, the modelling of C functions in hardware will be an achievable goal. As a designer, designed IRAD CPU board using Teledyne's multi-pipelined 7 gate-array chip set.

[redacted]

Consultants and Subcontracts.

There will be no consultants, all work will be done in house. There will be a subcontract to lease the XACT Development System. Total cost will be $1320.

Current and Pending Support.

The Imagination Works has no current or pending support at this time.

Pre-Existing Relevant Patents and Inventions.

The principal investigator has no patents at this time.

Potential Commercial Applications and Follow-on Funding Commitment.

The potential commercial applications are endless since the proposed computer can be reconfigured into any function. If the idea is a valid one, no doubt the computer will be used for things unthought of by its inventor. If Phase II is reached and a prototype is built there should be no problem with follow-on funding.

Equivalent Proposals

This proposal is to be submitted to both the NSF's and NASA's SBIR programs. The name on both proposals is "A Fully Programmable Reconfigurable Hardware Architecture Supercomputer". The date of submission of both is June 19, 1987. The name and title of the Principal Investigator is Steven M. Casselman, President of The Imagination Works.

For the NSF SBIR (address sent to: Data Support Services, National Science Foundation, 1800 G Street, N. W., Room 223, Washington, D. C. 20550, ATTN: SBIR) the solicitation number is 15d. The title is "New computing devices."

For the NASA SBIR (address sent to: SBIR Program Manager, Code IR, National Aeronautics and Space Administration, Washington, DC 20546) the solicitation number is 06.07. The title is "Computer Sciences Advances in Support of Computational Physics".

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APPENDIX C
(SEE INSTRUCTIONS ON REVERSE BEFORE COMPLETING)

SUMMARY PROPOSAL BUDGET

OMB No. 3145-0058
Exp. Date 11/31/88

ORGANIZATION	FOR NSF USE ONLY		
The Imagination Works	PROPOSAL NO.	DURATION (MONTHS) Proposed	Granted
PRINCIPAL INVESTIGATOR/PROJECT DIRECTOR: Steven M. Casselman	AWARD NO.		

A. SENIOR PERSONNEL: PI/PD, and Other Senior Associates (List each separately with title, A.6. show number in brackets)	NSF FUNDED PERSON-MOS. CAL.			FUNDS REQUESTED BY PROPOSER	FUNDS GRANTED BY NSF (IF DIFFERENT)
1. Steven M. Casselman	6			$ 28800	$
2. [redacted]	3			14400	
3.					
4.					
5. ( ) OTHERS (LIST INDIVIDUALLY ON BUDGET EXPLANATION PAGE)					
6. ( ) TOTAL SENIOR PERSONNEL (1-5)	9			43200	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. ( ) POST DOCTORAL ASSOCIATES					
2. ( ) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)					
3. ( ) GRADUATE STUDENTS					
4. ( ) UNDERGRADUATE STUDENTS					
5. ( ) SECRETARIAL-CLERICAL					
6. ( ) OTHER					
TOTAL SALARIES AND WAGES (A+B)				43200	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)					
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A+B+C)				43200	
D. PERMANENT EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $1,000.) (Do not use for Phase I)					
TOTAL PERMANENT EQUIPMENT					
E. TRAVEL 1. DOMESTIC (INCL. CANADA AND U.S. POSSESSIONS)					
2. FOREIGN (Do not use for Phase I)					
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $					
2. TRAVEL					
3. SUBSISTENCE					
4. OTHER					
TOTAL PARTICIPANT COSTS					
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES					
2. PUBLICATION COSTS/PAGE CHARGES					
3. CONSULTANT SERVICES					
4. COMPUTER (ADPE) SERVICES					
5. SUBCONTRACTS					
6. OTHER				1320	
TOTAL OTHER DIRECT COSTS					
H. TOTAL DIRECT COSTS (A THROUGH G)					
I. INDIRECT COSTS (SPECIFY)					
TOTAL INDIRECT COSTS					
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)					
K. Fee (If requested)					
L. Total Cost and Fee (J + K) (Not to exceed $50,000)				$ 44520	$

PI/PD TYPED NAME & SIGNATURE*	DATE	FOR NSF USE ONLY
INST. REP. TYPED NAME & SIGNATURE*	DATE	INDIRECT COST RATE VERIFICATION: Date Checked / Date of Rate Sheet / Initials - DGC / Program

NSF Form 1030 (4-83) *Supersedes All Previous Editions*

APPENDIX B

NSF 87-8

National Science Foundation
Small Business Innovation Research Program

PROJECT SUMMARY

NSF AWARD NO.

NAME OF FIRM
The Imagination Works

ADDRESS

18622 Saticoy Street
Reseda, California 91335

PRINCIPAL INVESTIGATORS (NAME AND TITLE)
Steven M. Casselman

TITLE OF PROJECT
A Fully Programmable Reconfigurable Hardware Architecture Supercomputer.

TOPIC TITLE	TOPIC NUMBER
NEW COMPUTING DEVICES	15 D

TECHNICAL ABSTRACT (LIMIT TO 200 WORDS)

The research proposed is investigation of a new approach into the area of supercomputing. With the advent of the programmable gate-array, [1] the possibility of mapping a software program directly into a large number of such devices implies a significant advance in the area of supercomputing. This ability to repeatably map software directly into a fully reconfigurable hardware architecture will minimize many of the problems facing conventional and parallel supercomputing such as memory fetch, microcode memory fetch, and sequencer decoding delay.

The research to be done will be two-fold:

1) Study the topology of the interconnection of arrays to find a way to allow a continuous plane of arrays to be created.

2) Write a compiler that will map a source code file into the proper binary format needed by the arrays.

KEY WORDS TO IDENTIFY RESEARCH OR TECHNOLOGY (8 MAXIMUM)
Supercomputer, Reconfigurable Hardware.

POTENTIAL COMMERCIAL APPLICATIONS OF THE RESEARCH

Commercial applications range from use in highly recursive mathematical and physical problems to high speed simulation of large systems.

APPENDIX A

EXHIBIT A

Proposal to the National Science Foundation
COVER PAGE

PROGRAM	PROGRAM SOLICITATION NO.: NSF 87-8
SBIR – SMALL BUSINESS INNOVATION RESEARCH	CLOSING DATE: JUNE 22, 1987

NAME OF SUBMITTING ORGANIZATION (AND LEGAL NAME IF DIFFERENT)

The Imagination Works

NAME OF ANY AFFILIATED ORGANIZATIONS (PARENT, SUBSIDIARY, PREDECESSOR)

None

ADDRESS OF ORGANIZATION (INCLUDE ZIP CODE)

18622 Saticoy St. Reseda Ca. 91335

TITLE OF PROPOSED PROJECT

A Fully Programmable, Reconfigurable, Hardware Architecture Supercomputer

REQUESTED AMOUNT	PROPOSED DURATION	PERIOD OF PERFORMANCE
$ 44,520	6 Months	January 1–June 30, 1988

TOPIC NO.	TOPIC TITLE	SUBTOPIC LETTER
15	NEW COMPUTING DEVICES	D

THE ABOVE ORGANIZATION CERTIFIES THAT:	YES	NO
1. It is a small business firm as defined on page 3.	X	
2. The primary employment of the principal investigator will be with this firm at the time of award and during the conduct of the research	X	
3. A minimum of two-thirds of the research will be performed by this firm in Phase I.		X
4. It qualifies as a minority and disadvantaged small business as defined on page 3.		X
5. It qualifies as a woman-owned small business as defined on page 3.		X
6. It will permit the government to disclose the title and technical abstract page, plus the name, address and telephone number of the corporate official if the proposal does not result in an award to parties that may be interested in contacting you for further information or possible investment.	X	
7. It will comply with the provisions of the Civil Rights Act of 1964 (P.L. 88-352) and the regulations pursuant thereto.	X	

PRINCIPAL INVESTIGATOR/ PROJECT DIRECTOR	COMPANY OFFICIAL (BUSINESS)	OTHER INFORMATION
NAME Steven M. Casselman	NAME Steven M. Casselman	YEAR FIRM FOUNDED 1985
SIGNATURE Steve Casselman	SIGNATURE Steve Casselman	NUMBER OF EMPLOYEES Avg. previous 12 mos. 1 Currently 2
SOCIAL SECURITY NO. OF PI/PD* [redacted]	TITLE President	PRESIDENT'S NAME Steven M. Casselman
DATE 06-19-87 TELEPHONE NO. 881-3291 Area Code: 818	DATE 06-19-87 TELEPHONE NO. 881-3291 Area Code: 818	HAS THIS PROPOSAL BEEN SUBMITTED TO ANOTHER AGENCY? Yes X No

* Submission of social security numbers is voluntary and will not affect the organization's eligibility for an award. However, they are an integral part of the NSF information system and assist in processing the proposal. SSN solicited under NSF Act of 1950, as amended.

Detailed breakdown of item 3.

Work Description	Time Allotted	Man-Hours*	Cost Incurred
1. Partition the C functions into groups whose implementation might be similar.	1 week	80	$2400
2. Pick simplest member of groups and translate into schematic capture system.	2 week	160	$4800
3. Simulate circuit and check for valid translation. Modify translation if necessary.	1 week	80	$2400
4. Implement remaining functions and enter in schematic capture.	1 month	320	$9600
5. Simulate and check for validity of translation.	2 weeks	160	$4800
6. Compile results and if time permits enter some short well known benchmark by translating the source code using the macros just created.	2 weeks	160	$4800
Total cost of Task 3		960	$28800

(* Mr. Barley working with P. I.)

Exhibit A.

Justification of Budget Request

The XACT Development System is the only equipment required to complete the proposed research. The Development System consists of:

Part Number	Description	Lease Cost/Month
LCA-MDS21	LCA Development System	$50
LCA-MDS22	LCA Simulator - P-SILOS	$50
LCA-MDS24	LCA In-Circuit-Emulator	$100
LCA-MDS25	LCA In-Circuit-Emulator Pod	$20
Total Cost of Equipment/Month		$220

This equipment will enable The Imagination Works to perform the proposed research in the given time frame. If used for six months the total cost will be $1320.

Detailed work schedule and estimated cost thereof.

Work Description	Time Allotted	Man-Hours	Cost Incurred
1. Initial Development kit Familiarization	2 weeks	80	$2400
2. Define the proposed architecture.	1 month	160	$4800
3. Implement C functions in hardware (see below)	3 months	800	$28800
4. Calculate percent Utilization	2 weeks	80	$2400
5. Calculate worst case timing	2 weeks	80	$2400
6. Prepare Final Report	2 weeks	80	$2400
Total cost for research manpower		1280	$43200

(cost per man-hour is $30, this includes salaries, wages, fringe benefits, and any overhead that might be incurred).